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PERFORMANCE ANALYSIS OF CACHE MEMORY DESIGN FOR SINGLE BIT ARCHITECTURE FOR ULTRA-LOW POWER

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ABSTRACT

In this paper, the design analysis of ultra-low-power cache memory design for single-bit architecture has been proposed and implemented. Cache Memory Design for Single Bit Architecture is composed of a circuit of the write driver circuit, six transistors static random access memory cell, and different types of sense amplifiers such as voltage differential sense amplifier, current differential sense amplifier, and charge transfer differential sense amplifier. Power reduction techniques are also applied over different blocks of architecture, such as sense amplifiers and six transistors static random access memory cells. The performance of different architectures has been analyzed in terms of power consumption, the number of transistors,and delay in sensing. The results depicted that single-bit six transistor static random access memory cell voltage mode differential sense amplifier architecture consumes 13.16µW of power, 12.5ηs delay in sensing, with 30 transistors compared to others. Furthermore, Process Corner Simulation and Monte Carlo Simulation also have been done to check the robustness of the circuit. The conclusion depicts that single bit six transistor static random access memory cell with power reduction sleep transistor technique voltage mode differential sense amplifier with power reduction sleep transistor technique in architecture consume 8.988 µW of power with 34 number transistors and lowest chip area 62.613× 30.48 mm2.

***KEYWORDS**: Six Transistor Static Random-Access Memory (6T-SRAM), Cache Memory Design for Single Bit Architecture (CMDSBA), Single Bit Six Transistor Static Random-Access Memory Current Differential Sense Amplifier Architecture (SB6TSRAMCDSAA), Single Bit Six Transistor Static Random Access Memory Charge Transfer Differential Sense Amplifier (SB6TSRAMCTDSAA),Single Bit Six Transistor Static Random Access Memory Voltage Differential Sense Amplifier (SB6TSRAMVDSAA).*

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